

A

B

C

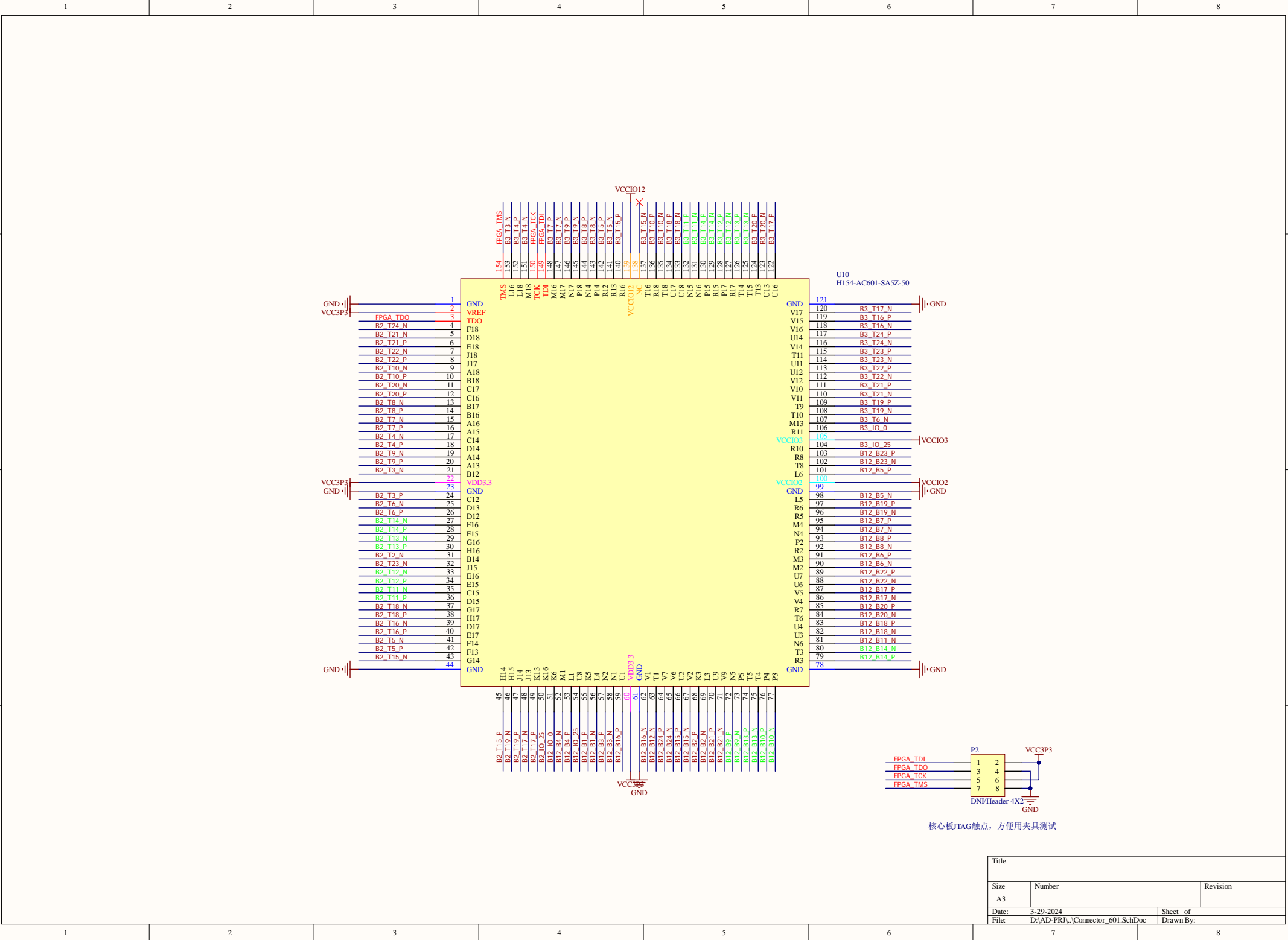
D

A

B

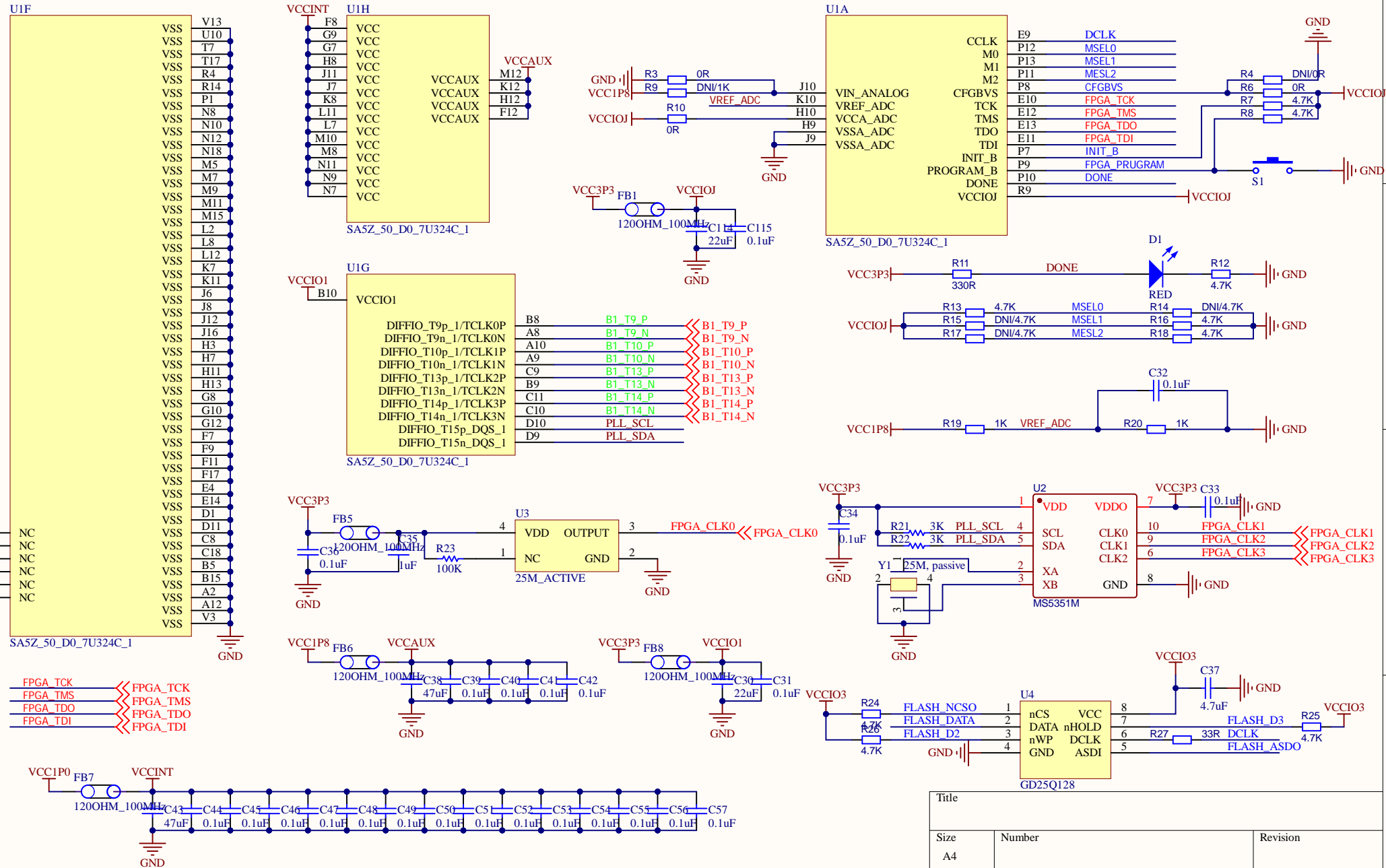
C

D

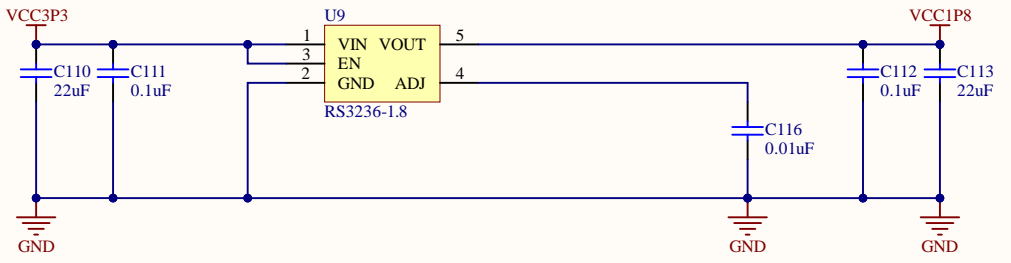
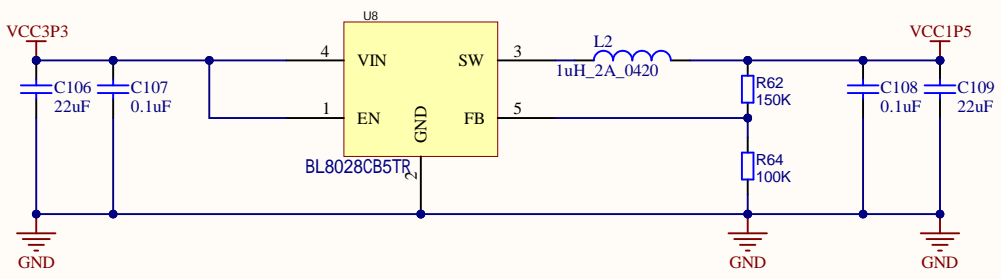
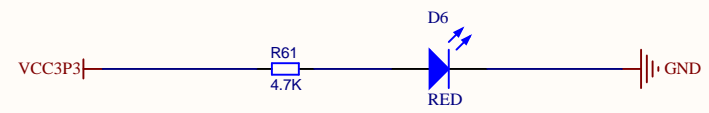
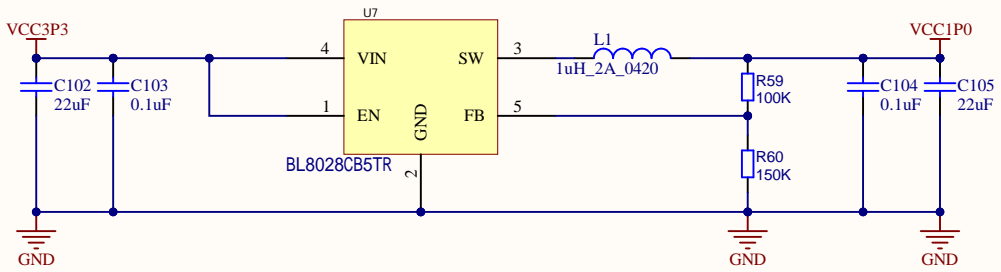


Title		
Size	Number	Revision
A3		
Date:	3-29-2024	Sheet of
File:	D:\AD-PRJ\...\Connector_601.SchDoc	Drawn By:





Title		
Size	Number	Revision
A4		
Date:	3-29-2024	Sheet of
File:	D:\AD-PRJ\...\FPGA_config.SchDoc	Drawn By:



Title		
Size	Number	Revision
A4		
Date:	3-29-2024	Sheet of
File:	D:\AD-PRJ\...\Power.SchDoc	Drawn By:



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A

A

B

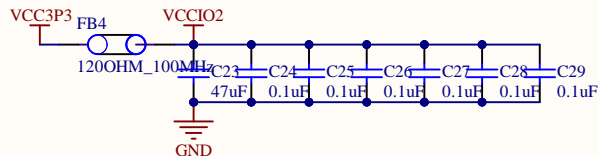
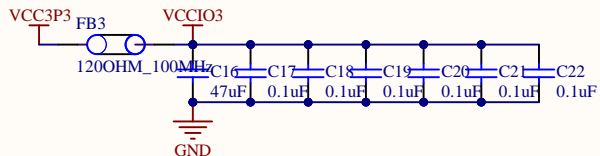
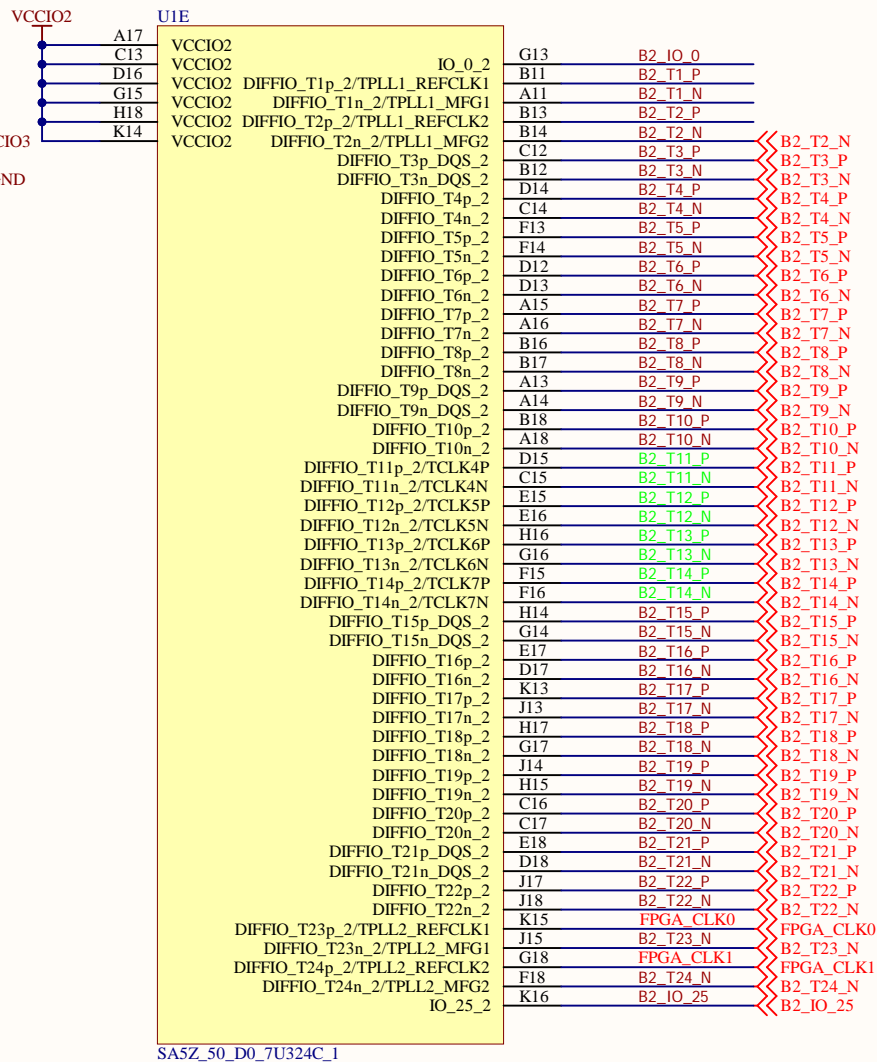
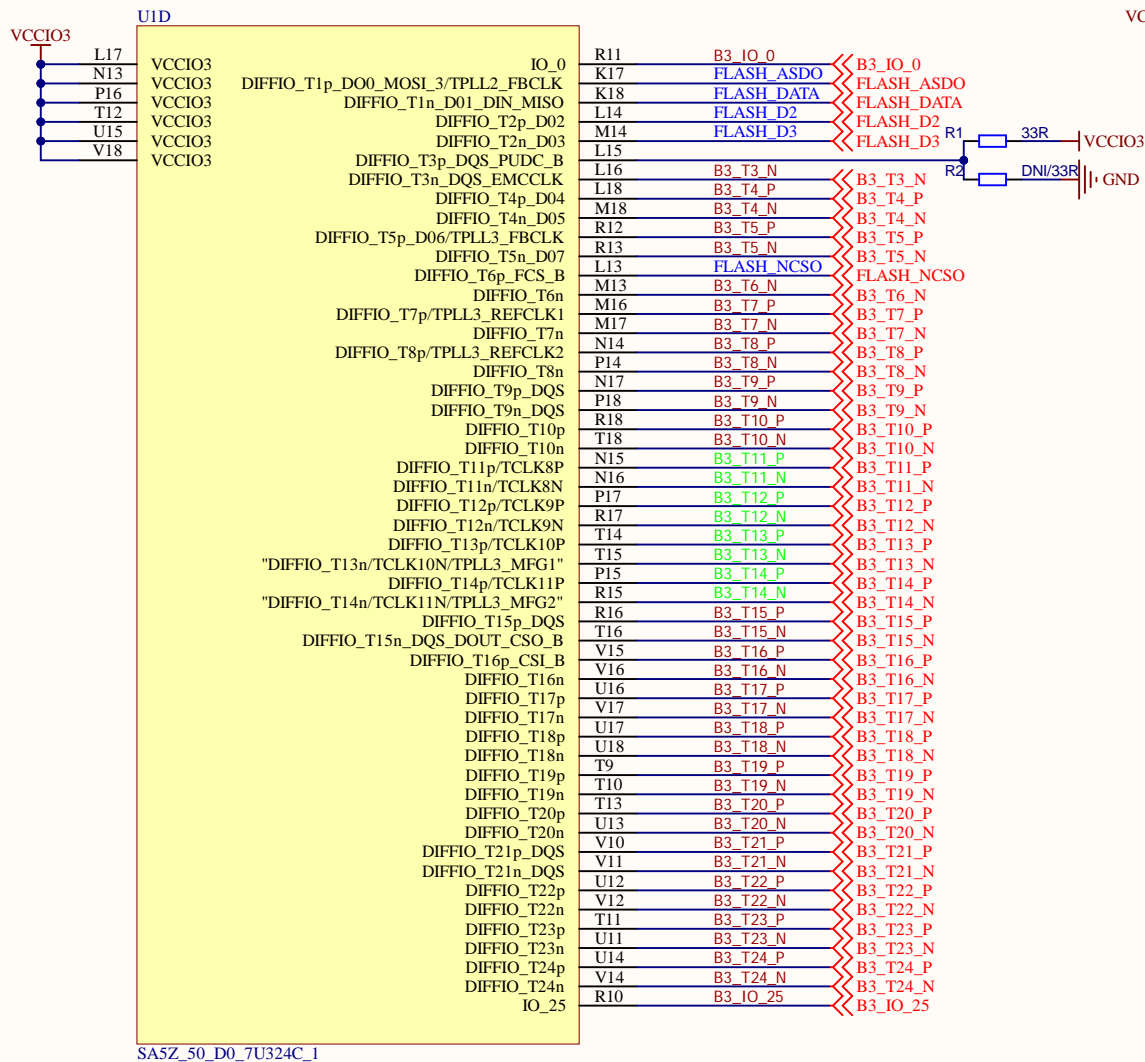
B

C

C

D

D



Title		
Size	Number	Revision
A4		
Date:	3-29-2024	Sheet of
File:	D:\AD-PRJ\SA5Z_50_D0_7U324C_2_SchDoc	Drawn By:

1

2

3

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