终极教程了已经
终极不是中级，前面的应用篇算中级，这个绝对是终极的
至少是某一个方向上的终极

这个方向就是：怎么用上容量更大的DDR条子，并且让它跑得更快？
容量大，跑得快，这还不是DDR里的高富帅吗？
有没有觉得这个叫法很合适呢？

好了现在开始吧

先明确概念
什么叫大？
什么叫快？

DDR3的条子现在最大是多大？32G？64G？
拜托，你以为是SD卡？
自己上淘宝去搜，至今（2013年12月13号）为止，最大的单根DDR条子就是8GB。
没有更大的了，淘宝上说16G的那是两根8G的DDR让你组双通道用的。

那什么叫快？你估摸着主时钟频率得500M吧？
500M？那是起步。
现在800M主时钟的都有了，折算一下就是1600M，淘宝关键词之一。
某些超频条子，比如海盗船，
号称能超到主频1000M以上，一般的FPGA怕是扛不住了。

从第二页开始，不卖关子了
高富帅的关键在于深度定制

这个定制当然在core gen的步骤里定制

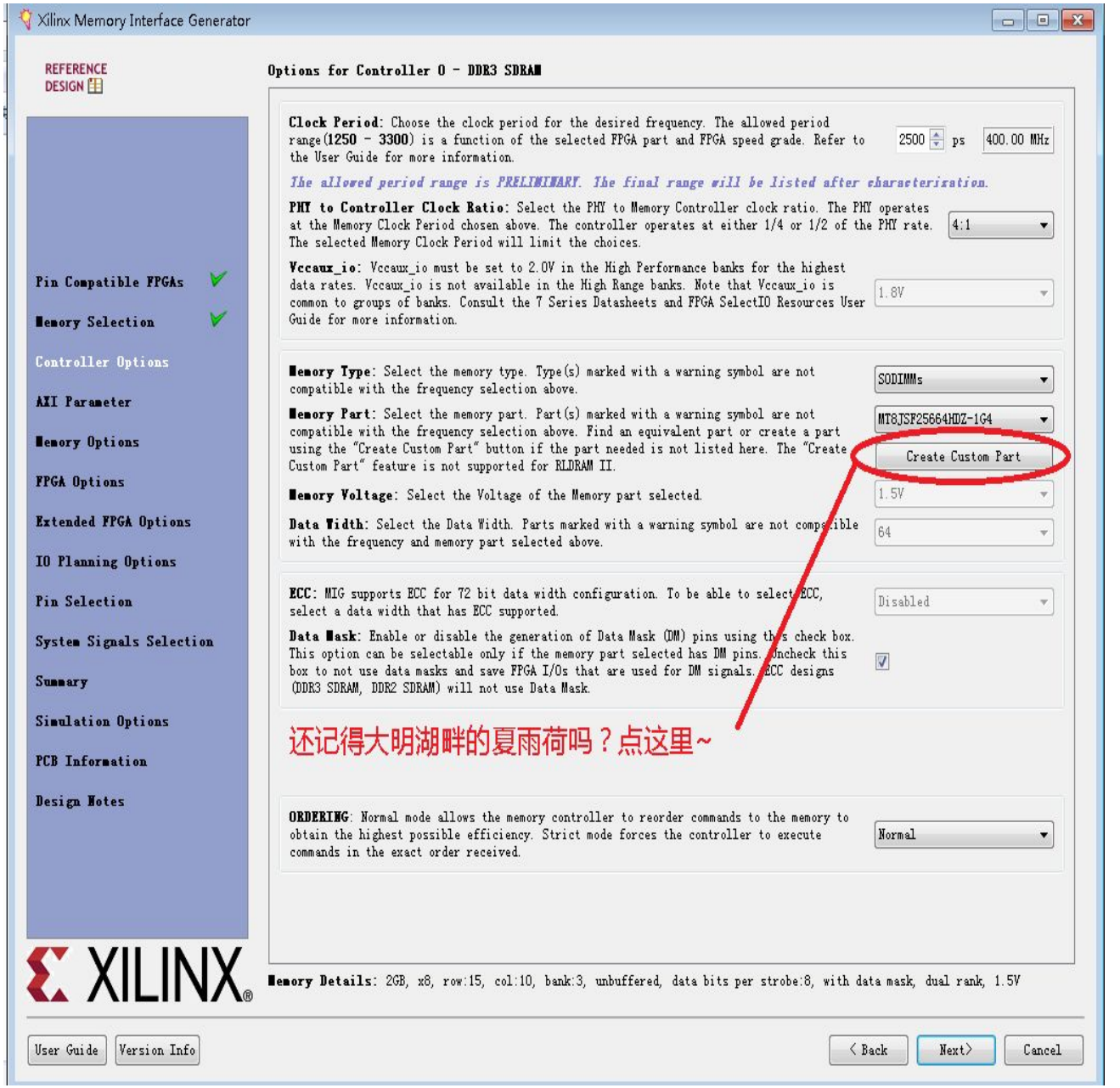
8G DDR3的条子在默认的设置下是没有的

这是为什么？

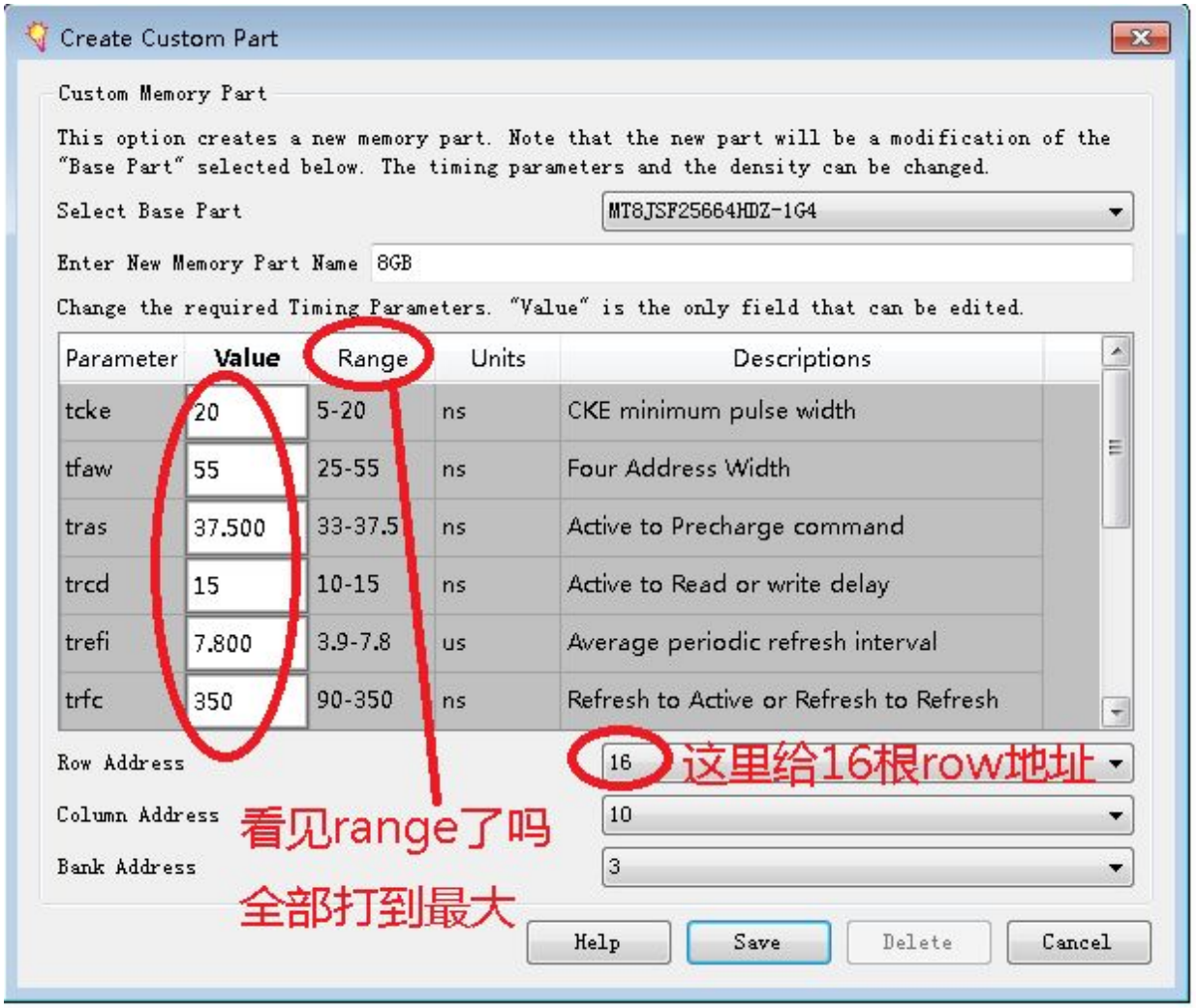
因为...一般人默认不用8G的条子。

那么你怎么定制呢？

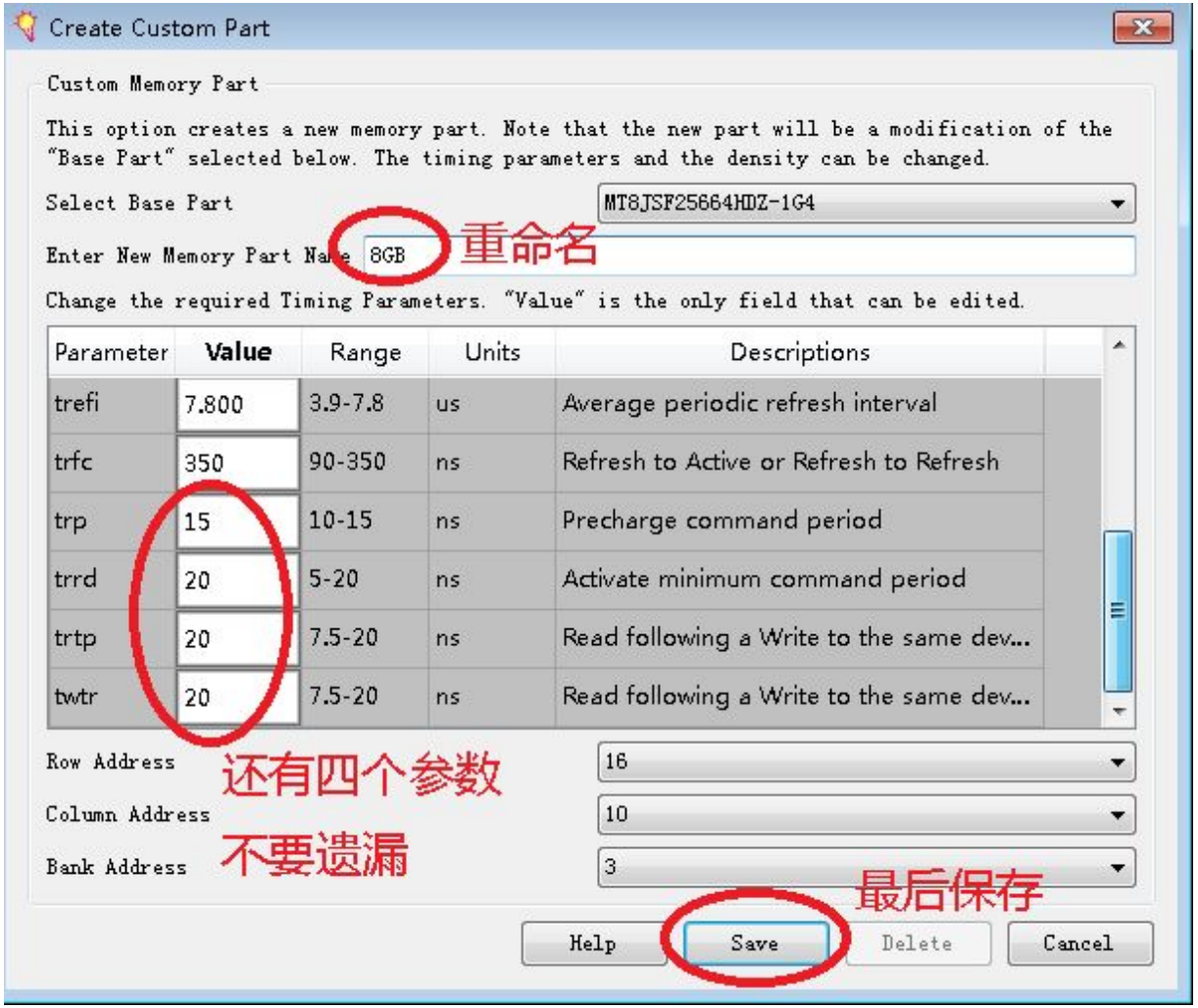
看右边的图

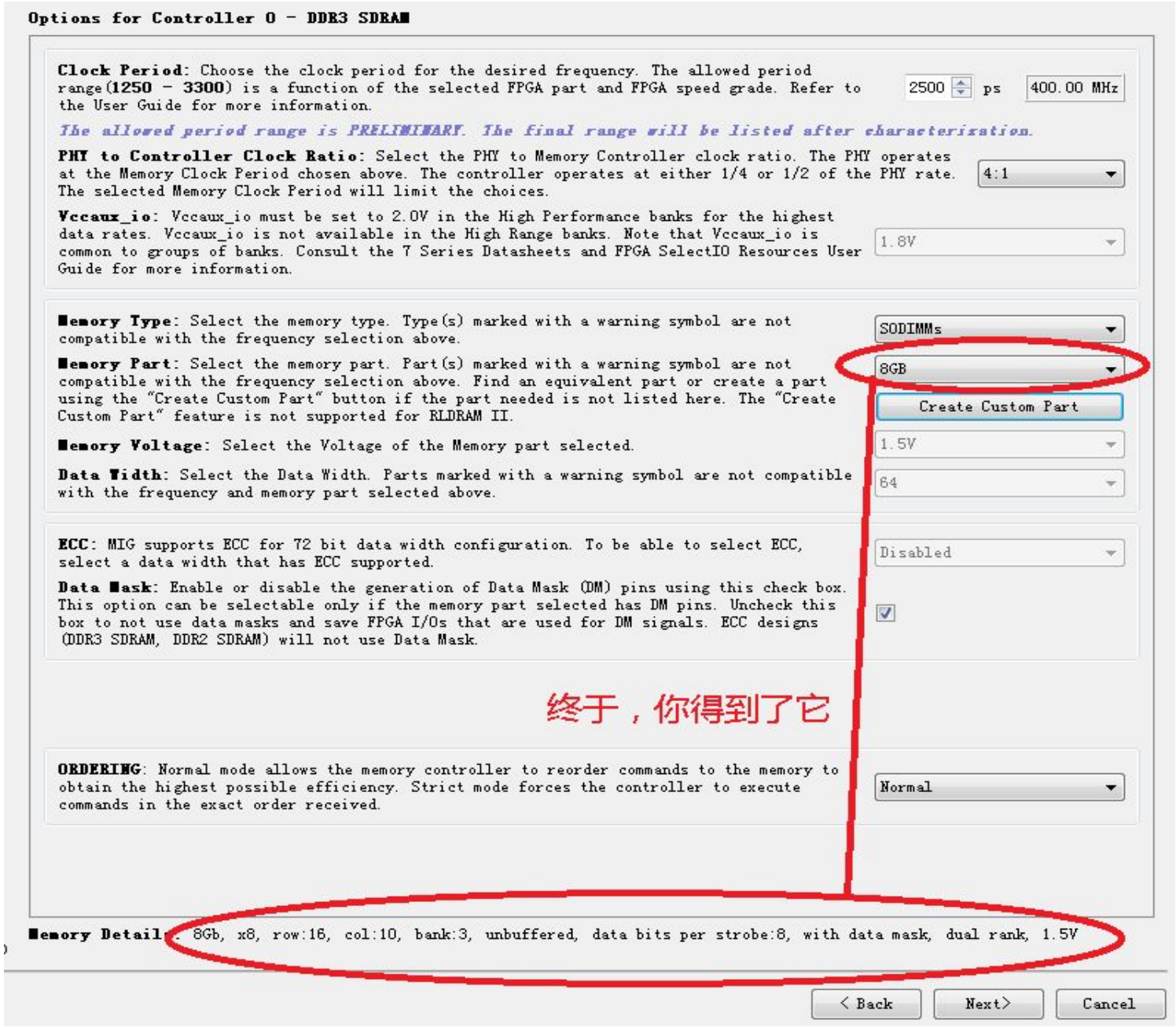


点进去就是这样，除了row地址改成16之外，还有第一页6个参数，全部给到最大值。



然后再这样，拉一下右边的拖动条，不要遗漏剩下的四个参数。
这样一共十个参数，全部打到最大值。




Options for Controller 0 - DDR3 SDRAM
Clock Period: Choose the clock period for the desired frequency. The allowed period range(1250 - 3300) is a function of the selected FPGA part and FPGA speed grade. Refer to the User Guide for more information.
2500 ps
400.00 MHz
The allowed period range is PRELIMINARY. The final range will be listed after characterization.
PHY to Controller Clock Ratio: Select the PHY to Memory Controller clock ratio. The PHY operates at the Memory Clock Period chosen above. The controller operates at either 1/4 or 1/2 of the PHY rate. The selected Memory Clock Period will limit the choices.
4:1
Vccaux_io: Vccaux_io must be set to 2.0V in the High Performance banks for the highest data rates. Vccaux_io is not available in the High Range banks. Note that Vccaux_io is common to groups of banks. Consult the 7 Series Datasheets and FPGA SelectIO Resources User Guide for more information.
1.8V
Memory Type: Select the memory type. Type(s) marked with a warning symbol are not compatible with the frequency selection above.
SODIMMs
Memory Part: Select the memory part. Part(s) marked with a warning symbol are not compatible with the frequency selection above. Find an equivalent part or create a part using the "Create Custom Part" button if the part needed is not listed here. The "Create Custom Part" feature is not supported for RLDRAM II.
8GB
Create Custom Part
Memory Voltage: Select the Voltage of the Memory part selected.
1.5V
Data Width: Select the Data Width. Parts marked with a warning symbol are not compatible with the frequency and memory part selected above.
64
ECC: MIG supports ECC for 72 bit data width configuration. To be able to select ECC, select a data width that has ECC supported.
Disabled
Data Mask: Enable or disable the generation of Data Mask (DM) pins using this check box. This option can be selectable only if the memory part selected has DM pins. Uncheck this box to not use data masks and save FPGA I/Os that are used for DM signals. ECC designs (DDR3 SDRAM, DDR2 SDRAM) will not use Data Mask.
终于，你得到了它
ORDERING: Normal mode allows the memory controller to reorder commands to the memory to obtain the highest possible efficiency. Strict mode forces the controller to execute commands in the exact order received.
Normal
Memory Details: 8Gb, x8, row:16, col:10, bank:3, unbuffered, data bits per strobe:8, with data mask, dual rank, 1.5V
< Back
Next>
Cancel

一个现象：你不改那十个参数的range，那是不行的
不改的话顶多只能支持2GB和4GB的条子跑上500M

8GB的条子上去就发现400M都跑不上

至于改了之后能跑多快...保守估计600M还是有的话，
看你电路板和FPGA的性能了。

至于为啥要改ROW地址...这貌似应用篇已经说过了...
下面是著名软件CPU-Z的截图，作为你改那十个参数的参考思路。

注意到参数越大频率越高没？

好了，8GB的条子，
金斯顿的就可以了
市场价五百块钱一根儿

注意别买到假货哦~